Remarks:

Reconsideration of the application is respectfully requested.

Claims 1 - 13 are presently pending in the application. Claim 1 has been amended to correct a grammatical error.

In item 9 of the above-identified Office Action, claims 1 - 5, 7 - 10, 12 and 13 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by U. S. Patent No. 6,477,674 to Bates et al ("**BATES**").

In item 10 of the Office Action, claim 6 was rejected under 35 U.S.C. § 103(a) as allegedly being obvious over **BATES** in view of U. S. Patent No. 6,704,897 to Takagi ("**TAKAGI**"). In item 11 of the Office Action, claim 11 was rejected under 35 U.S.C. § 103(a) as allegedly being obvious over **BATES** in view of U. S. Patent No. 5,751,151 to Levi et al ("**LEVI**").

Applicant respectfully traverses the above rejections.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Both independent claims of the present application require a semiconductor module including, among other limitations:

> "first and second equally sized groups of interface circuits, wherein each interface circuit of said first

group is assigned exactly one interface circuit of said second group;"

and

"a first circuit connected to said first group and serving to generate test signals to be multiplexed in and output via said interface circuits of said first group;

a second circuit connected to said second group for receiving and processing test signals received via said interface circuits of said second group; and"

As such, all claims of the instant application require, among other limitations: 1) **two groups of interface circuits, each interface circuit of the first group being assigned to exactly one respective interface circuit of the second group; 2)** that both groups of interface circuits are **equally sized,** (i.e., each group comprises the **same number of interface circuits** assigned to the other); and 3) **that a first circuit connected to said first group generates test signals, while a second circuit connected to said second group receives and processes the test signals.**

The **BATES** reference neither teaches nor suggests, among other limitations of Applicant's claims, Applicant's particularly claimed **first and second equally sized groups of interface circuits.** Rather, the **BATES** reference discloses a method and apparatus for conducting input/output loop back tests using a local pattern generator and delay elements. In a first

embodiment of **BATES**, an input/output (I/O) buffer 100 of Fig. 1 includes a test circuit 110. As stated in col. 2 of **BATES**, lines 38 - 41:

> "Additionally, I/O test circuit 110 receives the test signals after the signals have propagated through I/O buffer 100 and compares them to the data that was initially transmitted."

The embodiment of Fig. 1 of **BATES** discloses only a single I/O buffer 100. In figure 5 of **BATES**, cited on page 4 of the Office Action, there is shown a plurality of I/O buffers 100(1)-100(n). According to column 4 of **BATES**, lines 28 - 36:

> "FIG. 5 is a block diagram of one embodiment of an integrated circuit (IC) 500. IC 500 includes input/output (I/O) buffers 100(1)-100(n). **I/O buffers 100(1)-100(n) make up a data block of I/O circuitry for transmitting to and receiving data from other IC 100 devices.** According to one embodiment, a data block includes sixteen (16) I/O buffers 200. However, in other embodiments, a data block may include other multiples (e.g., 2, 4, 8, 12, 18, 32, 40, 64, etc.) of I/O buffers 100." [emphasis added by Applicant]

As noted above in the cited text, the **BATES** reference merely discloses that the I/O buffers 100(1)-100(n) communicate with **"other IC 100 devices"** (i.e., some further devices for receiving or transmitting the data), which seem to be pointed to in the Office Action on page 4 as allegedly analogous to Applicant's claimed **second group**. However, **BATES** does not particularly disclose much about these **"other IC 100 devices"**. For example, **BATES** does not disclose whether these **"other IC**

100 devices" are arranged in a second group of input/output buffers or if such a "second group" comprises the same number of input/output buffers as the first group, as is required by all of Applicant's claims. For example, the "other IC 100 devices" to which the I/O buffers 100(1)-100(n) of Fig. 5 of BATES are connected may actually include more I/O buffers than included in the "group" of input/output buffers 100(1)-10o(n), illustrated in Fig. 5 of BATES. Furthermore, a particular I/O buffer, arguendo, of BATES' undescribed "other IC 100 devices" in may not be assigned exclusively to one respective particular I/O buffer of the alleged "first group" of I/O buffers 100(1)-10(n) of BATES. More particularly, the BATES reference is silent on any details of the "other IC 100 devices" connected to the "first group" of I/O buffers 100(1)-10(n) of BATES and, thus, does not teach or suggest, among other things: 1) two groups of interface circuits, each interface circuit of the first group being assigned to exactly one respective interface circuit of the second group; and 2) that both groups of interface circuits are equally sized, as required by Applicant's claims.

More particularly, BATES doesn't explicitly disclose a second group of interface circuits, and thus, further doesn't teach or suggest the size of such second group and, in not discussing the second group or its size, BATES cannot possibly

be found to teach or suggest "**first and second equally sized groups**", as required by Applicant's claims. Additionally, in not explicitly disclosing a **second group** of interface circuits, **BATES** further fails to teach or suggest that "**each interface circuit of said first group is assigned exactly one interface circuit of said second group**". There is no information given in **BATES** regarding the number of "other IC 100 devices" to which the I/O devices 100(1)-100(n) connect, and thus **BATES** does not teach or suggest that each I/O device 100(1)-100(n) **is assigned exactly one interface circuit of the second group**, as required by Applicant's claims.

Further, **BATES** additionally fails to teach Applicant's claimed **first circuit** connected to said first group and generating **test signals**, with a **second circuit** connected to the second group to receive and process the **test signals**. Due to the failure of **BATES** to teach or suggest Applicant's particularly claimed first and second equally sized groups of interface circuits, the apparatus of **BATES** cannot be used for testing I/O buffers of a first group by means of I/O buffers of a second group, in accordance with the present invention. **Applicant's claimed invention needs the I/O buffers of a second group to compare data received from the first group to original data** (i.e., produced before transmission to the first group). Instead, the apparatus of **BATES** uses a compare unit

220 (Fig. 2 of **BATES**) located in the test unit 110 of the I/O buffer 100, itself, to compare data received from a particular I/O buffer 100(1)-100(n) (Fig. 5 of **BATES**) with original data supplied by the test pattern generator 210 (Fig. 2 of **BATES**). As stated in col. 3 of **BATES**, lines 19 - 20, "Fig. 2 is a block diagram of one embodiment of I/O test circuit 110.

Accordingly, the generated test data are sent to the compare unit 220 directly, via the "stage 215", and at the same time the generated test data is sent to the I/O buffer 100 of Fig. 1, which transmits the data via the amplifier 145 (see, col. 4 of **BATES**, lines 1 to 4) to a second input of the compare unit 220 (i.e., which is part of the test circuit 110 of Fig. 1). Accordingly, for testing purposes, in the system of **BATES**, the I/O buffer 100 disclosed in connection with Fig. 1 is not assigned or connected to any other I/O buffer (i.e., interface circuit) of any second group for testing purposes, since the I/O buffer 100 illustrated in Fig. 1 of **BATES**, is connected directly to the test pattern generator 210 and to the compare unit 220 of the test circuit 110, only. As can be seen from Fig. 1 of **BATES**, there is no second group of interface circuits (i.e. I/O buffers) receiving data from the buffer 100, to receive and process test signals from the first group.

Additionally, the semiconductor module of Applicant's claims requires, among other limitations:

> **"a respective separate voltage supply for said first and second groups of interface circuits."** [emphasis added by Applicant]

The **BATES** reference further fails to disclose that two groups of input/output buffers each with a respective separate voltage supply. In the Office Action, pad 140 of Fig. 1 of **BATES** is alleged to be an external reference voltage. However, only one single input/output buffer is disclosed in Fig. 1. Additionally, even if plural input/output buffers were disclosed, arguendo, in Fig. 1, disclosure of "separate voltage supplies is missing since the circumstance that the reference voltage is "external" does not mean that each input/output buffer would have a separate voltage supply line. Usually, each potential (like a reference potential) is supplied by only one single common supply line, which may be connected to plural sub-device structures within an integrated circuit. **BATES** fails to teach or suggest any departure from this standard rule, and thus fails to teach or suggest two groups of input/output buffers each including a respective separate voltage supply. As such, in the system of **BATES**, unlike Applicant's claimed system, the influence of voltage supplies of different groups of input/output buffers cannot be checked independently from each other.

Applicant's independent claim 7 further requires, among other limitations:

> "generating test signals, coupling in the test signals, and outputting the test signals via the first group of interface circuits;
>
> receiving the test signals via the second group of interface circuits; and
>
> comparing the received test signals with prescribed values for fault-free functioning of the interface circuits."

As such, independent claim 7 requires, among other limitations, **sending test signals** from a first group of interface circuits (i.e., arguendo, to input/output buffers 100(1)-100(n) of **BATES**) to a second group of interface circuits (which, as stated above, is not explicitly taught in **BATES**). **BATES** neither teaches nor suggests Applicant's particularly claimed receipt in a second group of test signals from a first group. Rather, as noted above, **BATES**, in col. 4, lines 30 - 32, states:

> "I/O buffers 100(1)-100(n) make up a data block of I/O circuitry for transmitting to and receiving data from other IC 100 devices." [emphasis added by Applicant]

However, when referring to testing of the apparatus of **BATES**, which occurs in connection with the embodiment of Fig. 2, test data is transmitted from the tested input/output buffer to the test circuit 100 of Fig. 1 (i.e., to the compare unit 220 of

Fig. 2 of **BATES**) rather than to any other input/output buffers.

In view of the foregoing, the **BATES** reference neither teaches, nor suggests, all limitations recited in Applicant's claims 1 and 7 of the instant application. Neither the further cited **TAKAGI** reference, nor the further cited **LEVY** reference, make up for the shortcomings in the **BATES** reference.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claims 1 and 7. Claims 1 and 7 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 1 or 7. As it is believed that the claims were patentable over the cited art in their original form, the claims have not been amended to overcome the references.

In view of the foregoing, reconsideration and allowance of claims 1 - 13 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a

telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

Kerry P. Sisselman
Reg. No. 37,237

For Applicant

KPS:cgm

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Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101